SIMPLIFICATION OF HORMONICS AND ENHANCEMENT OF POWERFACTOR BY USING BUCK PFC CONVERTER IN NON LINEAR LOADS

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ABSTRACT:

The devices generally used in industrial, commercial and residential applications need to undergo rectification for their proper functioning and operation. They are connected to the grid comprising of non-linear loads and thus have non-linear input characteristics, which results in production of non-sinusoidal line current. Also, current comprising of frequency components at multiples of line frequency is observed which lead to line harmonics. Due to the increasing demand of these devices, the line current harmonics pose a major problem by degrading the power factor of the system thus affecting the performance of the devices. Hence there is a need to reduce the line current harmonics so as to improve the power factor of the system. This has led to designing of Power Factor Correction circuits. In this paper we designed an active Power factor circuit using Buck converter for improving the Power Factor.

An improved constant ON time control is proposed to operate in critical conduction mode (CRM).And to eliminate the dead zones in Ac input current by adding an auxiliary switch and two diodes. With optimal control parameters, nearly unit power factor can be achieved. Moreover, the efficiency of the proposed converter is not deteriorated compared to the conventional buck converter. When the result are verified by using MATLAB/SIMULINK.

INTRODUCTION

Nowadays, most ac/dc power converters are forced to reduce the harmonic current to meet the some special power products such as lighting equipment's Power factor correction (PFC) is a good method for providing an almost sinusoidal input current. The boost converter is the most popular topology for PFC applications due to its inherent current shaping ability [1]–[2]. However, with universal input, usually a 400 Vdc output voltage is required for the Boost PFC. The boost PFC cannot achieve high efficiency at low line input because it works with large duty

cycle in order to get high-voltage conversion gain. Therefore, it is hard to increase the power density of boost PFC converter due to the thermal concern at low line input.

THE Sepic converter [3], [4] and quadratic buck-boost [5], [6] can achieve high power factor (PF) and reduce the output voltage stress. But the voltage stress of switch in these two topologies is much higher than that in the boost PFC converter that reduces the efficiency and increases the cost. In this paper, an improved buck PFC converter is proposed, as shown in Fig.1. Compared with the conventional buck PFC converter, an auxiliary switch and two diodes are added in the improved buck PFC converter. The proposed converter has two different operation modes in a line period. When the input voltage is higher than the output voltage, the proposed converter operates in buck mode, which is same as the conventional buck converter. When the input voltage is lower than the output voltage, the proposed converter operates in buck-boost mode. The buck PFC converter has some attractive merits. First, the output voltage of buck converter is always regulated lower than the boost converter. Second, the voltage across the main switch of the buck converter is almost clamped to the input voltage. Therefore, the buck PFC converter can achieve relatively high efficiency within the universal input voltage range and it has drawn more and more attention in the past years [7]How-ever, if the buck converter operates in hard switching mode, the switching loss especially at high input will be large, which deteriorates the merit of the buck converter . The buck dc–dc converter operating in critical continuous conduction mode (CRM) can eliminate the reverse recovery loss in diode and achieve zero voltage switching (ZVS) for the switch The constant ON-time (COT) control for CRM buck PFC converter is introduced in With COT control, the peak current in the switch is almost proportional to the input voltage, and then high PF can be achieved.

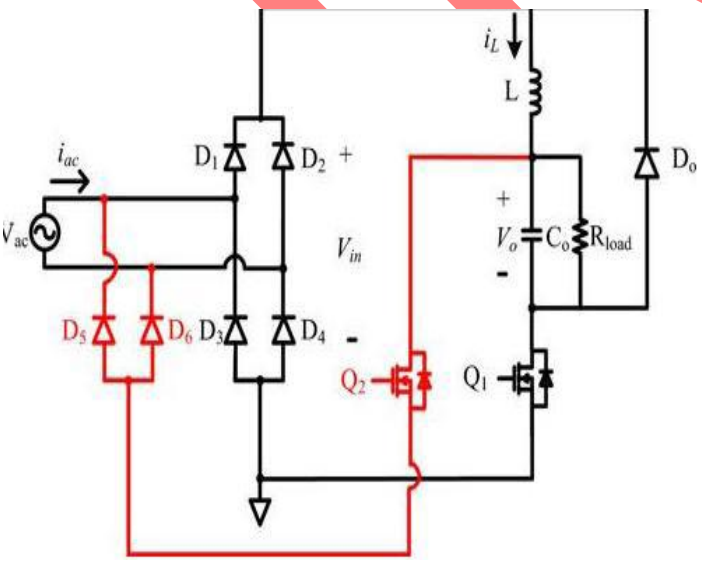

Fig. 1.Proposed improved buck PFC converter

II. PRINCIPLE OF OPERATION

In the proposed converter operates in CRM will be analysed in detail. To simplify the analysis, the transitions between the switches and the output diode *Do* are omitted. After that, there still exist eight operation stages in a line period. Fig. 2 shows the equivalent circuits of the stages easy into it.

A. Positive Buck-Boost Operation Mode

When the input voltage *V*ac is in positive half cycle and the magnitude of *V*ac is smaller than V_o the proposed converter operates in buck-boost mode. During this mode, switch Q_1 keeps OFF and switch Q_2 keeps switching. There are two stages when the proposed converter operates under this

Mode:

Stage 1: When switch Q_2 is ON, the proposed converter operates in stage 1. The equivalent circuit of this stage is shown in Fig. 2(a). The inductor L is charged by V_{ac} through D_1 and D_6 and i_L increases during this stage

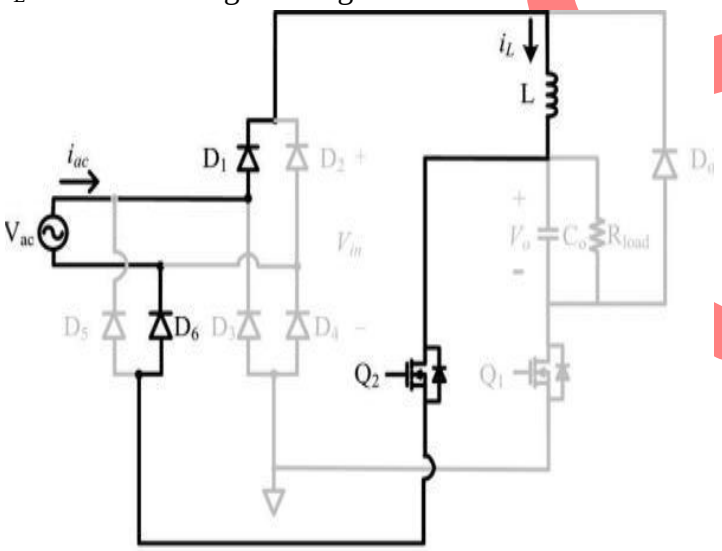

Fig: 2(a) Equivalent circuits of the proposed converter in First stages

Stage 2:

When switch Q_2 is OFF, the proposed operates in stage 2. The equivalent circuit of this stage is shown in Fig. 2(b). The inductor L is discharged by V_o through D_o and i_L decreases during this stage converter

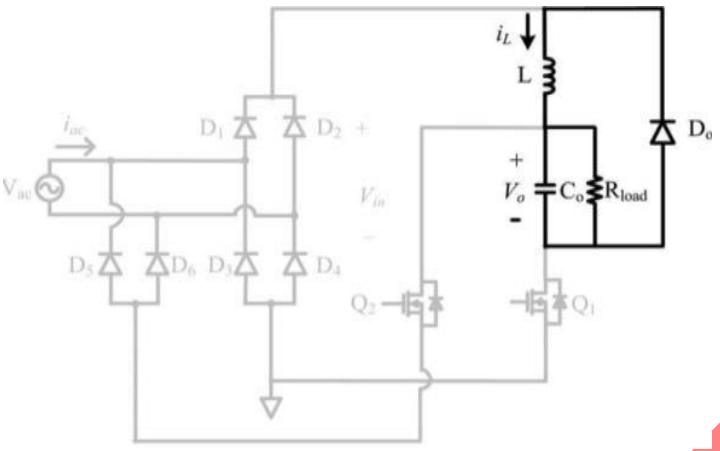

Fig: 2(b) Equivalent circuits of the proposed converter in Second stages

B. Positive Buck Operation Mode:

When the input voltage *V*ac is in positive half cycle and the magnitude is larger than *Vo*, the proposed converter operates in buck mode. During this mode, switch Q_2 keeps OFF and Switch Q_1 keeps switching. There are two stages when the proposed converter operates under this mode *Stage* 3:

When switch Q_1 is ON, the proposed converter operates in stage 3. The equivalent circuit of this stage is shown in Fig. 2(c). The inductor *L* is charged by *V*ac−*Vo* through D_1 and D_4, and i_L increases during this stage.

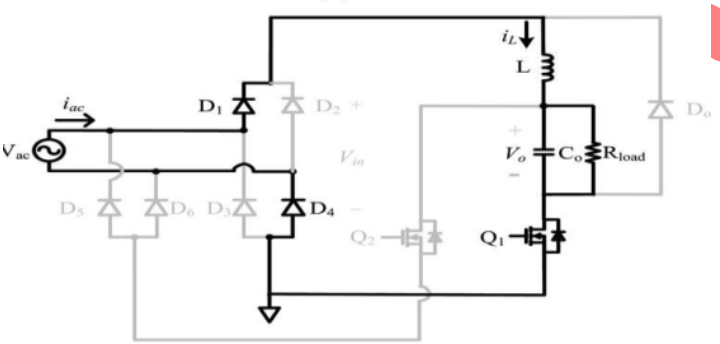

Fig: 2(c) Equivalent circuits of the proposed converter in Third stages

Stage 4:

When switch $Q_1$is OFF, the proposed converter operates in stage4.The equivalent circuit of this stage is same as that stage 2, as shown in the Fig.2 (b).The inductor L is discharge by v_o through Do and i_L decreases during this stage.

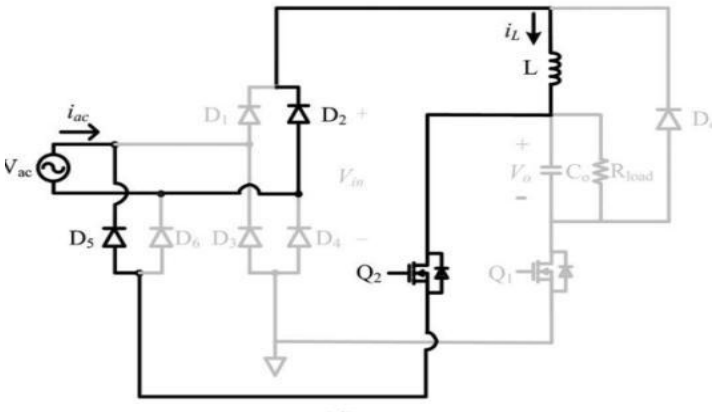

Fig: 2(d) Equivalent circuits of the proposed converter in five stages

The inductor *L* is discharged by *Vo* through Diode *Do* and this section, the proposed converter operates in CRM will be analyzed in detail. To simplify the analysis, the transitions between the switches and the output diode *Do* are omitted. After that, there still exist eight operation stages in a line period. Fig. 2 shows the equivalent circuits of the stages be separated into four operation stages defined as stages 5–8, and the equivalent circuits include Fig. 2(b), (d), and (e). The negative half cycle operation processes of the proposed converter are similar to those of the positive half cycle. For simplicity, the negative operation processes are not depicted in detail here.

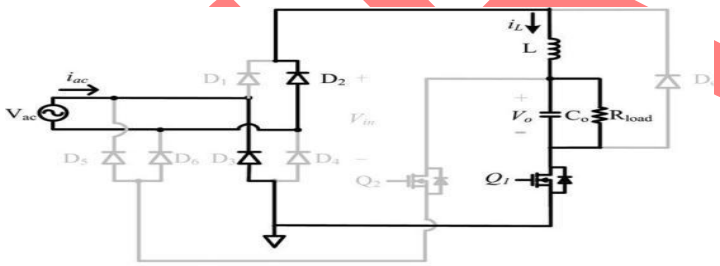

Fig: 2(e) Equivalent circuits of the proposed converter in six stages

III. SCHEMATIC OF THE PROPOSED BUCK PFC CONVERTER WITH AN IMPROVED COT CONTROL

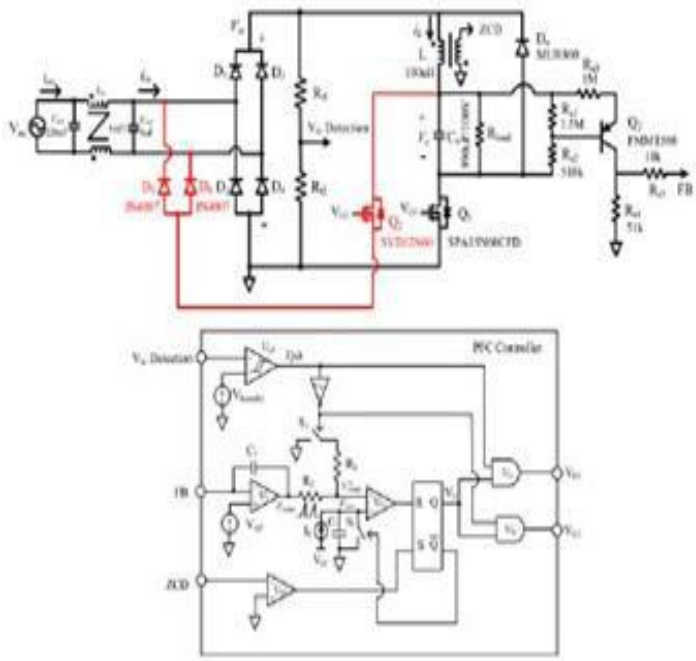

Fig.3. Schematic of the proposed buck PFC converter with an improved COT control

An improved COT control is applied for the proposed buck PFC converter to force it that operates in CRM, as shown in Fig. 3. The output voltage is detected with a level-shift circuit formed by a high-voltage transistor *Q*2 and the resistors *Ra1~Ra4*. Some key waveforms are shown in Fig. 4. As shown in Fig. 3, the control signal *V*ph used to control the converter either in buck mode or buck boost mode is achieved by comparing the detected *V*in signal *V'*in with a voltage reference *V*boundry. Usually, *V*boundry is set to reflect the output voltage *Vo* with the same ratio as that *V'*in reflects *V*in . *V*ph is high logic when *V'*in is higher than *V*boundry and is low logic when *V'*in is lower than *V*boundry the detected output signal V_{FB} is sent to the negative input of the error amplifier U_f.

The error between V_{FB} and the set reference V_{ref} is amplified by the compensation networks C_f and an amplified error signal *V*comp is achieved. The dc voltage signal *V'*comp applied to control the conduction period TON is achieved from *V*comp through a control networks formed by resistors R_1 and *R*2 and switch S_1. Switch *S*1 is controlled by the control signal *V*ph. The proposed converter operates in buck mode whenS_1 is OFF and operates in buck-boost mode when S_1 is ON. *V'*comp is a step function controlled by V_{ph}, as shown in (1).

V'comp= {

V_{COMP} $V_{IN} > V_0$

$K*V_{COMP}$ $V_{IN} <= V_O$

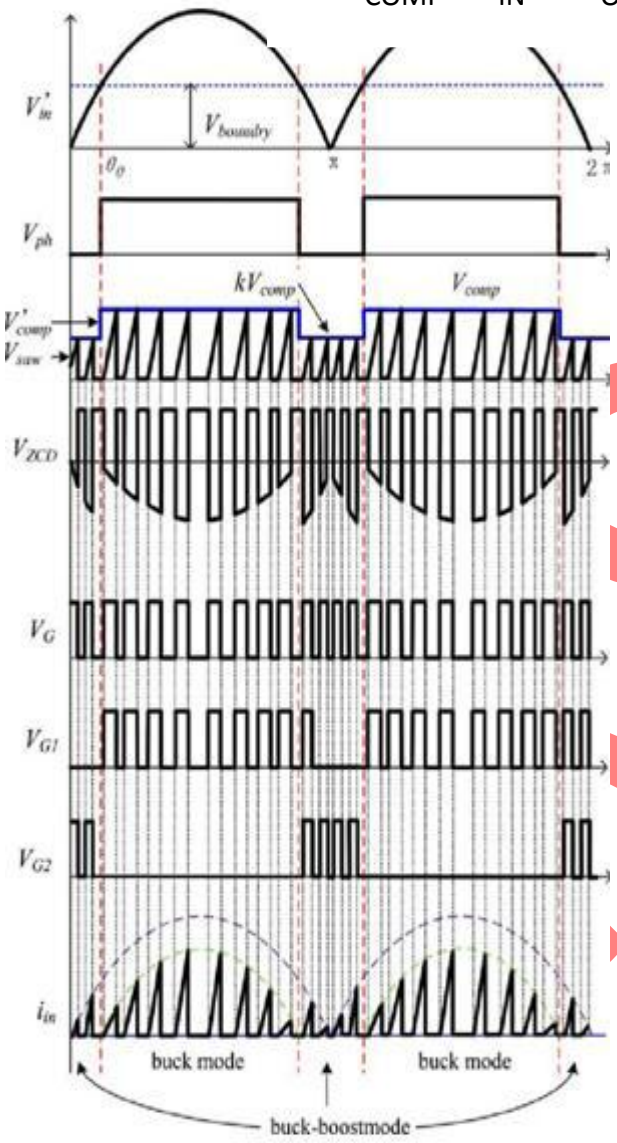

Fig. 4. Key waveforms in the improved COT control diagram.

This level transition sets the driving signal from low level to high level According to the aforementioned analysis; the rising slope of V_{saw} is constant due to the constant current sourcei_1 charging during the whole line period. Therefore, the ON-time (*T*ON) of the switches is determined by *V'*comp proportionally. Smaller value of *k* leads to smaller T_{ON} and smaller peak values of i_L when the proposed converter is operating in buck-boost mode. As shown in Figs.3and 4. The driving signals V_{G1} and V_{G2} are controlled by V_{ph} for the different

operation modes alternately. Different coefficient k results in the different PF correction performance and the overall efficiency. Where k is a coefficient equal to $R1/(R1+R2)$. Similar to the conventional COT control, a constant current source i_1. CapacitorC_1, and switch $S_2$are used to generate a saw tooth wave form V_{saw}. When V_{saw} reaches V'_{comp}, the output of comparator U_{c1} jumps from low level to high level.

IV. SIMULATION RESULTS

A. CONVENTIONAL CIRCUIT:

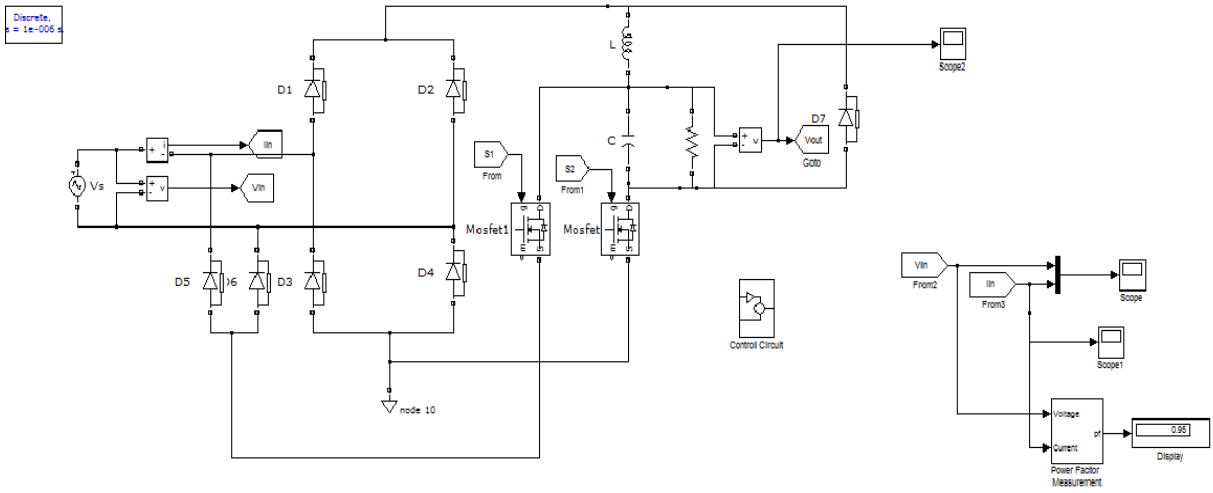

Fig 5. Conventional Circuit Buck PFC Converter with High Power Factor

This level transition results the driving signal from high level to low level. The zero-crossing point of the inductor current i_L is detected by the auxiliary winding of the inductor L. This inductor current zero-crossing detection signal V_{ZCD} can be applied in both buck and buck-boost modes. When the inductor current i_L falls to zero, the output voltage auxiliary winding V_{ZCD} starts to fall. Once VZCD falls to zero, the output of comparator U_{c2}jumps from low level to high level. This level transition sets the driving signal from low level to high level.

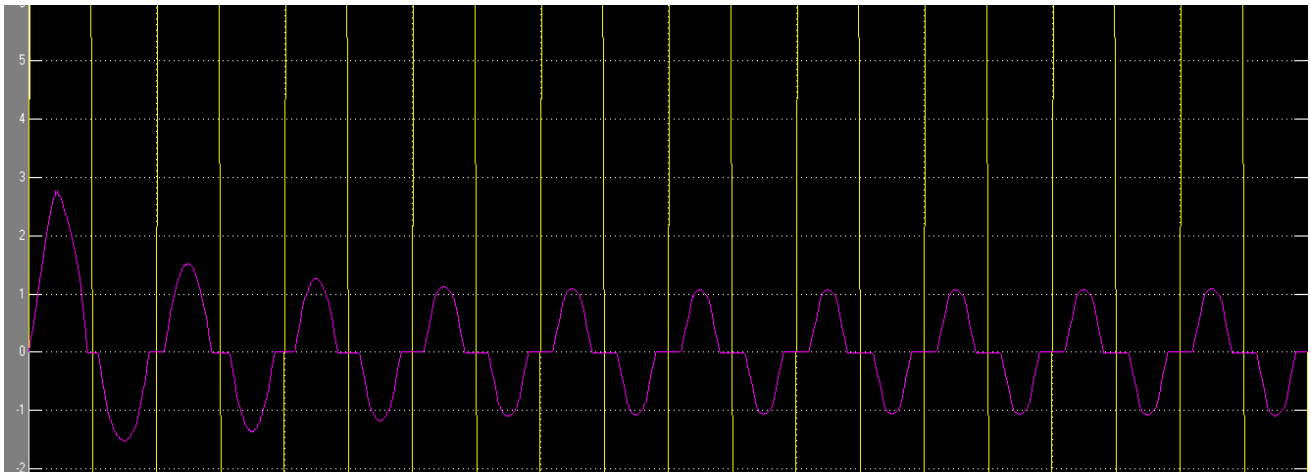

Fig6. Measured input voltage and input current waveforms

B. PROPOSED CIRCUIT:

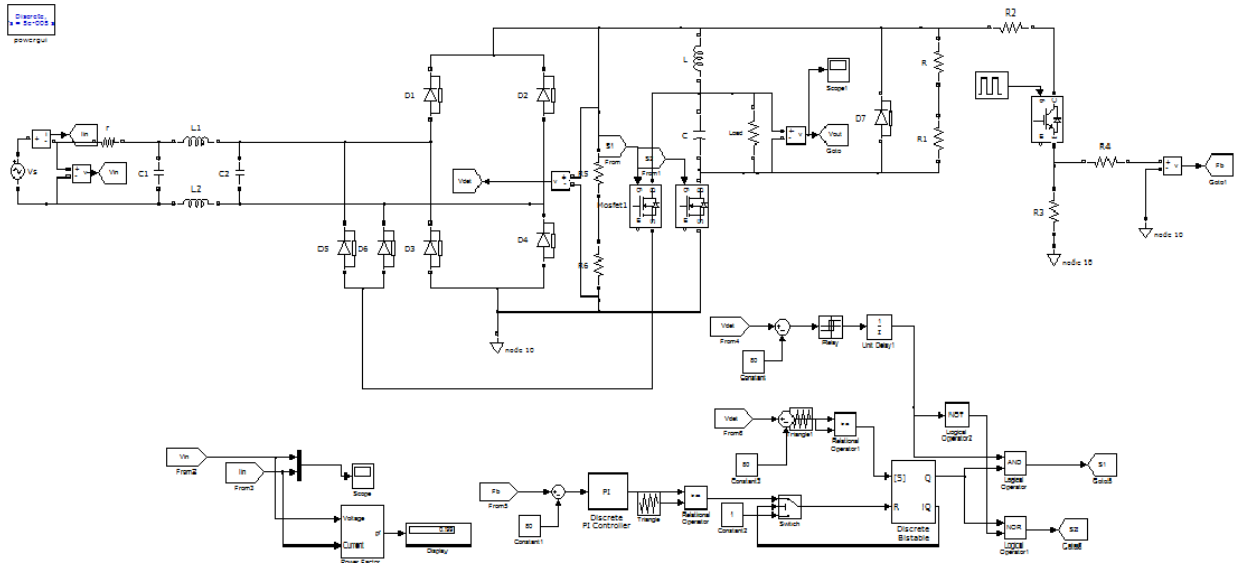

Fig **7.** Proposed Circuit Buck PFC Converter with High Power Factor

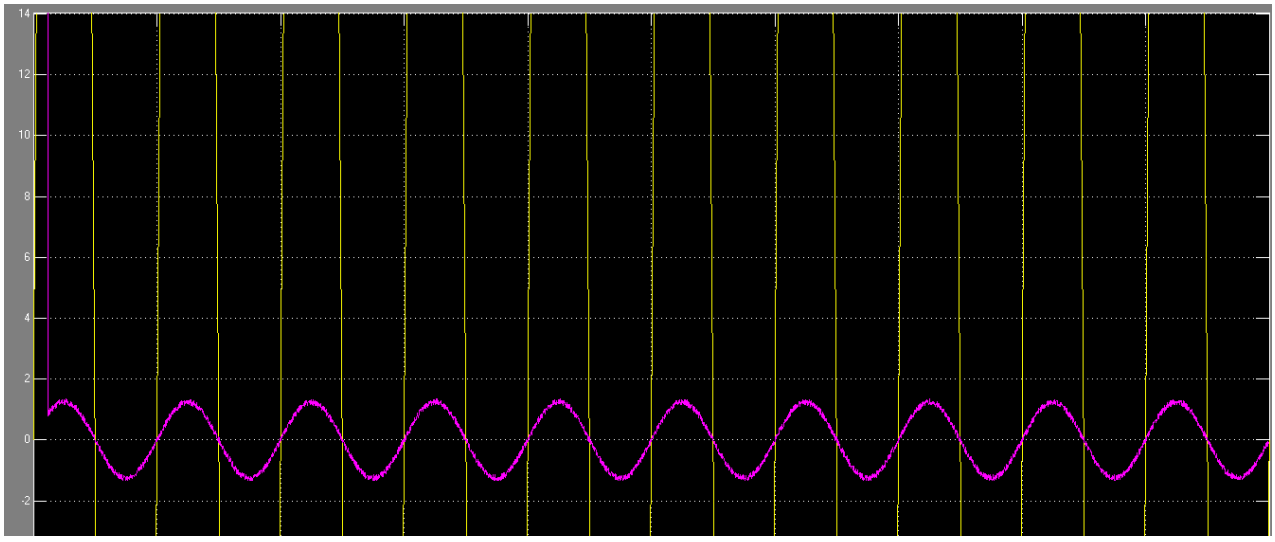

Fig 8.Measured input voltage and input current waveforms of the proposed converter (90 Vac and full load).

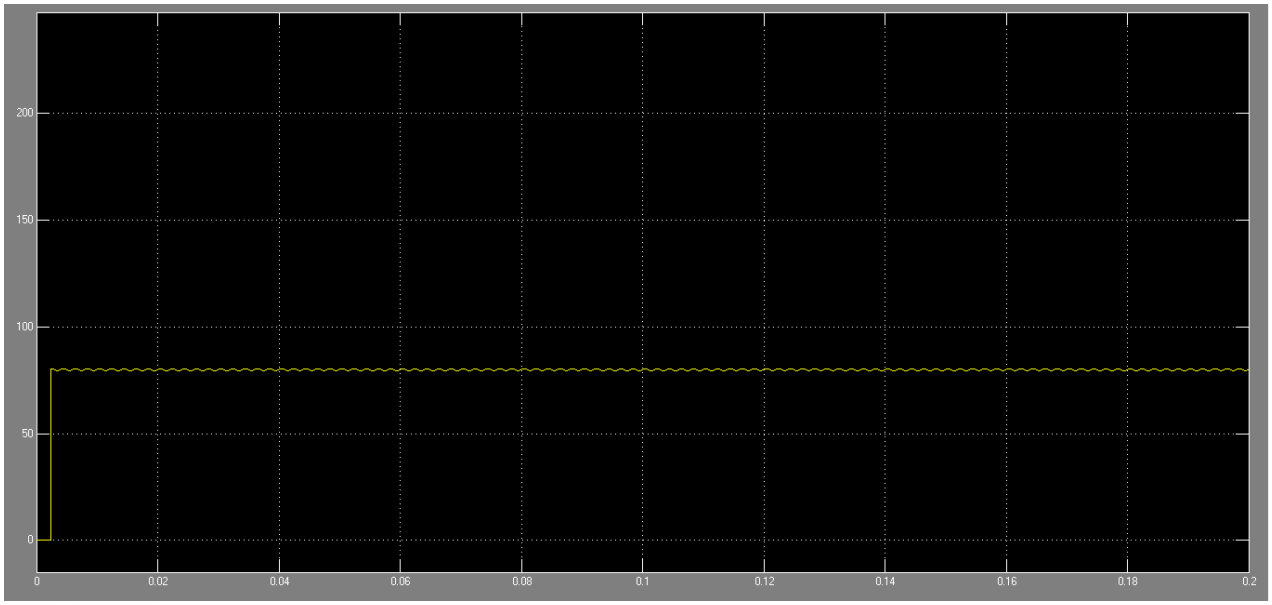

Fig.9 Output voltage waveform at load side

V. CONCLUSION

The improved buck PFC converter topology proposed in this paper to improve the power factor upto unity, by reducing the harmonics that while we are managed that the system is operated in critical conduction mode by improving C.O.T. from this we are eliminated the dead zones. Hence the power factor achieves nearly unity by converting non linear characteristics into linear characteristics.

REFERENCES

[1] Electromagnetic Compatibility (EMC), Part 3-2: Limits–Limits for Harmonic Current Emissions (Equipment Input Current≤1A Per Phase), International Standard IEC 61000-3-2, 2005,

[2] E. L. Huber, B. T. Irving, and M. M. Jovanovich, "Effect of switching and switching-frequency limitation on line-current distortions of DCM/CCM boundary boost PFC converters," IEEE Trans. Power Electron., vol. 24, no. 2, pp339–347, Feb. 2009

[3] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduce components and conduction losses," IEEE Trans. Ind. Electron.vol.58, no. 9, pp. 4153–4160, Sep. 2011.

[4] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," IEEE Trans. Ind. Electron., vol. 56, no.4, pp. 1147–1157, 2009

[5]M.A.AlSaffar,E.H.Ismail,andA.J.Sabzali,"Integrated buck–boost quadratic buck PFC rectifier for universal input applications,IEEETrans.Power Electron., vol. 24, no. 12, pp.2886–2896, Dec. 2009.

[6] J. M. Alonso, J. Vi˜na, D.Gacio, L. Campa, G. Mart´ınez, and R.Osorio, "Analysis and design of the quadratic buck-boost converter as a high-power- factor driver for power-LED lamps,"in Proc. IEEE IECON, Nov.2010, pp 2541–2546.

[7] H. Endo, T. Yamashita, and T. Sugiura, "A high-power-factor buck converter," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun./Jul.1992, pp. 1071–1076.